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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,225	FORBES, LEONARD	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed November 11, 2004. Claims 1-38 are pending, in which claims 37-38 have been newly added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 37, meaning and scope of "that the body region is not formed across other surfaces" are unclear and indefinite, since it is lacking proper antecedent basis for "other surfaces", and unclear "other surfaces" of which region or layer?.

Claim Rejections - 35 USC § 103

2. Claims 1-26,37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazure et al (5,308,782) taken with Mukai (5,804,848) and Colinge (Article of "Reduction of Kink Effect...").

Mazure teaches (at Figs 1-14; col 3, line 1 through col 8) a method for forming a transistor on a substrate comprising at least the main steps of: forming a silicon on insulator (SOI) including an insulating layer on the substrate (col 3, lines 1-10); forming a first source/drain region 28 on the substrate (col 4, lines 26-55); vertically forming a body region on the first source/drain region, wherein vertically forming the body region 30 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 4 and 9; col 4, line 56 through col 5, line 44), wherein full channel region depletion is desired in order to achieve improved performance (col 14, lines 57-68); forming a second source/drain region 32/34 on the body region 30; forming a first gate 18/19 on a first one of the opposing sidewall surfaces with a first gate oxide 22 therebetween; forming a second gate 18 on a second oxide of the second one of the opposing sidewall surfaces with a second gate oxide 22 therebetween (Figs 4 and 9-10), wherein forming first source/drain region by ion implantation or epitaxial growing (col 4, lines 36-55). Re claims 31-36, wherein by forming a silicon on insulator (SOI), an insulating layer is formed between the body region and on the substrate (col

3, lines 1-10). Re claim 37, insofar as understood, opposite sidewall surfaces of the body region 30 are not formed across each of other surfaces (Figs 4 and 9). Re claim 38, wherein as the width of the body region is sufficient thin to make the transistor as a fully depleted structure (col 14, lines 57-68), wherein a minimum lithographic feature size of 0.25 micron is mentioned at column 7, lines 3-20), and wherein due to such thin width of the body region relative to the doping concentration and fully depleted structure, the threshold voltage is inherently insensitive to fluctuations in the doping concentration.

Re base claims 1,8,9,13,14,20, Mazure lacks mentioning thickness of the body region as a fully depleted structure with thin width relative to a doping concentration such that a bulk charge is negligible in transistor operation.

However, Colinge teaches to form a thin film transistor comprising a thin body channel region as fully depleted structure (page 97, left column; page 99), wherein the body region a doping concentration (NA) and having a thin width thickness of about 100 nm that is sufficiently thin relative to the doping concentration such that a bulk charge (QB) has negligible effect in transistor operation, inherently. Mukai teaches (at Figure) forming a plurality of gate electrode including a first gate on a first one of the opposing sidewall surfaces, and a second gate on a second one of the opposing sidewall surfaces (Fig 15; col 1, lines 15-42; and Figs 1A,2-4, col 3-4), wherein the gate electrodes (23a-23d, 15a,15b) are independently of each other and applying a bias to the channel region in the body region 21 on one side of the gate electrodes (col 1, lines 37-42; col 2, lines 1-4; col 1, line 10-14; col 4, lines 7-18), that is coupling the first and second the gate electrodes to a first voltage source and second voltage source through a contact, respectively.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure having from one to N conductive gate electrodes by operating the gate electrodes independently of each other and applying a bias to the channel region on one side of the gate electrodes, that is coupling the first and second the gate electrodes to a first voltage source and second voltage source through a contact, respectively, as taught by Mukai. This is because of the desirability to independently operate the gate electrodes independently each from the other, wherein the bulk charge (QB) can have a negligible effect in transistor operation due to low doping concentration and a thin width

of the body region. Also it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure to have a thin thickness as taught by Colinge so as to form the thin film transistor comprising a thin body channel region operated as fully depleted structure, and to form a very thin transistor, wherein full channel region depletion is desired by Mazure in order to achieve improved performance (Mazure at col 14, lines 57-68). Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of thickness, as taught by the references including Mazure and Colinge, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, see In re Aller, etal., 105 USPQ 233; In re Waite 77 USPQ 586 (CCPA 1948); In Re Swanson 56 USPQ 372 (CCPA 1942).

3. Claims 1-30,37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,060,746) taken with Mukai (5,804,848).

Bertin et al teach a method (Figs 6,7,3A-9; cols 4-6) for forming a transistor on a substrate comprising at least the main steps of: forming a first source/drain region on the substrate; vertically forming a body region 19 on the first source/drain region 23,12 (Figs 6,7) as a fully depleted structure (col 2, lines 17-21), wherein the body region has a low doping concentration (NA) and a thin width thickness that is sufficiently thin relative to the low doping concentration such that a bulk charge (QB) has negligible effect in transistor operation, inherently, wherein vertically forming the body region 19 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 6,7; col 4, line 65 through col 5); forming a second source/drain region 22 on the body region; forming a first gate 15 on a first one of the opposing sidewall surfaces with a first gate oxide 18 therebetween (col 6); forming a second gate 15 on a second oxide 18 of the second one of the opposing sidewall surfaces with a second gate oxide therebetween, wherein forming first source/drain region by ion implantation, epitaxial growing or combination thereof (col 3, lines 40-47), wherein the body channel region having a thickness of 0.18 micron (col 2, lines 43-60), wherein the body region is encased with a ASG film and then annealing to diffuse the N-type dopant (col 5, lines 20-67), wherein CVD depositing and employing a BSG film as well known

in the art for providing P-type dopant would have been obvious to one of ordinary skill in the art. Re claim 37, insofar as understood, opposite sidewall surfaces of the body region 19 are not formed across each of other surfaces (see Figs 6,7). As the width of the body region is desired to be sufficient thin to make the transistor as a fully depleted structure (col 2, lines 10-21; col 4, lines 26-37), wherein less than the minimum dimension definable by lithography, and due to such thin width of the body region relative to the doping concentration and fully depleted structure, the threshold voltage is inherently insensitive to fluctuations in the doping concentration (re claim 38).

Berlin lacks mentioning the bias of the first gate and second gate.

However, Mukai teaches forming a plurality of gate electrode including a first gate on a first one of the opposing sidewall surfaces, and a second gate on a second one of the opposing sidewall surfaces (Fig 15; col 1, lines 15-42; and Figs 1A,2-4, col 3-4), wherein the gate electrodes (23a-23d, 15a,15b) are independently of each other and applying a bias to the channel region in the body region 21 on one side of the gate electrodes (col 1, lines 37-42; col 2, lines 1-4; col 1, line 10-14; col 4, lines 7-18), that is coupling the first and second the gate electrodes to a first voltage source and second voltage source through a contact, respectively, and there is a case of applying an equal voltage to each of the gate electrodes 23a-23d (col 5, lines 35-38, lines 28-38; col 4, lines 7-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure having from one to N conductive gate electrodes by operating the gate electrodes independently of each other and applying a bias to the channel region on one side of the gate electrodes or applying an equal voltage to each of the gate electrodes, that is coupling the first and second the gate electrodes to a first voltage source and second voltage source of the same through a plurality of contacts, respectively, as taught by Mukai. This is because of the desirability to supply a voltage source to the gate electrodes and biasing.

4. Claims 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,060,746) taken with Mukai (5,804,848), as applied to claims 1-30 and further of Mazure et al (5,308,782).

Bertin et al teach a method (at Figs 6,7,3A-9; cols 4-6) for forming a transistor on a substrate as applied to claims 1-30 above.

The references including Berlin lack forming an insulating layer on the substrate,

However, Mazure teaches (at col 3, lines 1-10) forming a transistor on a substrate, wherein the substrate includes a bulk silicon substrate or a silicon on insulator (SOI) substrate including a silicon layer on an insulating layer on a silicon substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Berlin on a silicon on insulator (SOI) substrate including an insulating layer on a silicon substrate as taught by Mazure, because these alternative substrates are art recognized alternative for substitution, wherein substrate capacitance is reduced due to the insulating layer formed on the silicon substrate.

Response to Amendment

*** Applicant's remarks filed November 01, 2004 have been considered but they are not persuasive, and in moot of the new ground(s) of rejection.

*** Applicant remarked that "Applicant cannot find in Mazure et al...forming a fully depleted body region having a width and doping concentration as recited in claim 1..."

In response, this is noted and found unconvincing. First, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Second, claim 1 does not recite any value for the width. The limitations of "width is sufficiently thin relative to a doping concentration" and "negligible" are merely relative terms. Although the "bulk charge" is negligible in operation, the bulk charge still has a value by mathematic calculation.

Contrary to Applicant's remark about "cannot find in Mazure et al...", Mazure clearly teaches (at col 14, lines 57-68) about forming the body region having a width that is sufficient thin to make the transistor as a fully depleted structure (col 14, lines 57-68), wherein a minimum lithographic feature size of 0.25 micron is mentioned at column 7, lines 3-20). Due to such very thin width (very small Wd value) of the body region relative to the doping concentration (NA) with fully depleted structure, the value of QB =q NA Wd is very small. Then, accordingly, the

threshold voltage does not depend strong on bulk charge (QB), and be negligible in transistor operation due to such very thin width of the body region of the fully depleted transistor.

*** Applicant remarked that "Applicant cannot find in Bertin et al...forming a fully depleted body region having a width and doping concentration as recited in claim 1...".

In response, this is noted and found unconvincing. Bertin et al clearly teach (at col 2, lines 10-21) that "very narrow diameter pillar makes fully depleted operation possible. Fully depleted operation mode is desirable as it provides enhanced gate control...", wherein "the vertical embodied by pillars having a diameter which is less than the minimum dimension definable by lithography (i.e., smaller than minimum image size on a mask)". Due to such very thin width (Wd) of the body region relative to the doping concentration (NA) and fully depleted structure, the value of QB =q NA Wd is very small, then the threshold voltage does not depend strong on bulk charge (QB), and be negligible in transistor operation due to thin width of the body region of the fully depleted transistor.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-7

Michael Trinh
Primary Examiner